In the Claims

Please amend the claims as follows:

Claims 1 to 43 (Canceled)

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44. (Currently Amended) A single integrated circuit comprising:

a first data processor including

a first program counter (2903) storing an address of a next instruction,

a first opcode register (2911) storing a current instruction,

first data processing units (2902, 2905, 2906, 2907, 2908, 2909, 2910) capable of data processing,

a first control logic (2904) connected to said opcode register for control of said first data processing units corresponding to said current instruction stored in said first opcode register according to a first instruction set;

a second data processor including

a second program counter (3100) storing an address of a next instruction,

a second opcode register (3105) storing a current instruction,

second data processing units (3301, 3302, 3303, 3304) capable of data processing,

a second control logic (3002) connected to said opcode register for control of said second data processing units corresponding said current instruction stored in said second opcode register according to a second instruction set, said second ~~instruction set~~ data processing units having a

different mapping of instructions to controlled operations than that of said first instruction set; and

B1 an external interface (11) connected to said first and second data processors and adapted for connection to memory (15) external to said single integrated circuit, said external interface forming the only connection between said first and second data processors and memory external to said single integrated circuit;

where said first and second data processors are capable of independent operations on disjoint instructions and data sets.

Claim 45. (Canceled)

46. (Previously Added) The single integrated circuit of claim 44, wherein:

said first data processor further includes a first data register file (2901) connected to said first data processing units for temporarily storing data; and

said second data processor further includes a second data register file (3300) connected to said second data processing units for temporarily storing data.

47. (Currently Amended) The single integrated circuit of claim 44, further comprising:

a first read/write memory connected to said first data processor and to said second data processor, whereby said first processor ~~is~~ and said second data processor are each capable of reading from ~~or~~ and writing to said first read/write memory; and

a second read/write memory connected to said second data processor, whereby said second data processor is capable of reading from ~~or~~ and writing to said second read/write memory and said first data processor is not capable of either reading from or writing to said second read/write memory.

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Claim 48. (Canceled)

49. (Previously Added) The single integrated circuit of claim 44, wherein:

said first data processor is a digital signal processor (DSP); and

said second data processor is a reduced instruction set computer (RISC) processor.

Claims 50 and 51. (Canceled)

52. (Currently Amended) A single integrated circuit comprising:

a first data processor including

a first program counter (2903) storing an address of a next instruction,

a first opcode register (2911) storing a current instruction,

first data processing units (2902, 2905, 2906, 2907, 2908, 2909, 2910) capable of data processing,

a first control logic (2904) connected to said opcode register for control of said first data processing units corresponding to said current instruction stored in said first opcode register according to a first instruction set;

a first read/write memory connected to said first data processor, whereby said first processor is capable of reading from ~~or~~ and writing to said first read/write memory;

a first instruction memory connected to said first data processor storing instructions in said first instruction set, said first data processor operating in accordance with instructions in said first instruction set recalled from said first instruction memory;

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a second data processor including

a second program counter (3100) storing an address of a next instruction,

a second opcode register (3105) storing a current instruction,

second data processing units (3301, 3302, 3303, 3304) capable of data processing,

a second control logic (3002) connected to said opcode register for control of said second data processing units corresponding said current instruction stored in said second opcode register according to a second instruction set, said second ~~instruction set~~ data processing units having a different mapping of instructions to controlled operations than that of said first instruction set;

a second read/write memory connected to said second data processor, whereby said second processor is capable of reading from ~~or~~ and writing to said second read/write memory;

a second instruction memory connected to said second data processor storing instructions in said second instruction set, ~~said~~ said second processor operating in accordance with instructions in said second instruction set recalled from said second instruction memory; and

an external interface (11) connected to said first and second data processors and connectable to ~~devices~~ memory (15) external to said single integrated circuit, said external interface forming the only connection between said first and second data processors and memory external to said single integrated circuit;

where said first and second data processors are capable of independent operations on disjoint instructions and data sets.

53. (Previously Added) The single integrated circuit of claim 52, wherein:

said first data processor further includes a first data register file (2901) connected to said first data processing units for temporarily storing data; and

said second data processor further includes a second data register file (3300) connected to said second data processing units for temporarily storing data.

54. (Previously Added) The single integrated circuit of claim 52, wherein:

said first data processor is a digital signal processor (DSP); and

said second data processor is a reduced instruction set computer (RISC) processor.

Claims 55 and 56. (Canceled)

57. (New) The single integrated circuit of claim 47, wherein:

said first data processor is operable to generate a request for data movement to or from said first read/write memory;

said second data processor is operable to generate a request for data movement to or from said first read/write memory and for data movement to or from said second read/write memory;

said external interface is operable to receive a request for data movement from said first data processor and from said second data processor and to move data responsive thereto.

58. (New) The single integrated circuit of claim 57, wherein:

each request for data movement generated by said first data processor or generated by said second data processor includes an indication of source address, an indication of destination address and an indication of amount of data; and

said external interface is operable upon receipt of said request for data movement to move said indicated amount of data from said indicated source address to said indicated destination address.

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59. (New) The single integrated circuit of claim 57, wherein:

said first read/write memory is operable to prioritize requests for access with said first data processor having a highest priority, said second data processor having an intermediate priority and said external interface having a lowest priority.

60. (New) The single integrated circuit of claim 52, wherein:

said first data processor is operable to generate a request for data movement to or from said first read/write memory;

said second data processor is operable to generate a request for data movement to or from said first read/write memory and for data movement to or from said second read/write memory;

said external interface is operable to receive a request for data movement from said first data processor and from said second data processor and to move data responsive thereto.

61. (New) The single integrated circuit of claim 60, wherein:

each request for data movement generated by said first data processor or generated by said second data processor includes an indication of source address, an indication of destination address and an indication of amount of data; and

said external interface is operable upon receipt of said request for data movement to move said indicated amount of data from said indicated source address to said indicated destination address.

62. (New) The single integrated circuit of claim 57, wherein:

said first read/write memory is operable to prioritize requests for access with said first data processor having a highest priority, said second data processor having an intermediate priority and said external interface having a lowest priority.

63. (New) A single integrated circuit comprising:

a first data processor including

a first program counter (2903) storing an address of a next instruction,

a first opcode register (2911) storing a current instruction,

first data processing units (2902, 2905, 2906, 2907, 2908, 2909, 2910) capable of data processing,

a first control logic (2904) connected to said opcode register for control of said first data processing units corresponding to said current instruction stored in said first opcode register according to a first instruction set;

a second data processor including

a second program counter (3100) storing an address of a next instruction,

a second opcode register (3105) storing a current instruction,

second data processing units (3301, 3302, 3303, 3304) capable of data processing,

a second control logic (3002) connected to said opcode register for control of said second data processing units corresponding said current instruction stored in said second opcode register according to a second instruction set, said second instruction set units having a different mapping of instructions to controlled operations than that of said first instruction set;

a read/write memory connected to said first data processor and said second data processor whereby both said first data processor and said second data processor are each capable of reading from and writing to said read/write memory;

an external interface (11) connected to said first data processor, said second data processors and adapted for connection to memory (15) external to said single integrated circuit, said external interface forming the only connection between said first data processor and said second data processors and memory external to said single integrated circuit, wherein said first data processor and said second data processor are each capable of generating a request for data movement to or from said read/write memory and said external interface is operable to receive a request for data movement from said first data processor and from said second data processor and to move data responsive thereto; and

wherein said first and second data processors are capable of independent operations on disjoint instructions and data sets.

64. (New) The single integrated circuit of claim 63, wherein:

said first data processor further includes a first data register file (2901) connected to said first data processing units for temporarily storing data; and

said second data processor further includes a second data register file (3300) connected to said second data processing units for temporarily storing data.

65. (New) The single integrated circuit of claim 63, wherein:

each request for data movement generated by said first data processor or generated by said second data processor includes an indication of source address, an indication of destination address and an indication of amount of data; and

said external interface is operable upon receipt of said request for data movement to move said indicated amount of data from said indicated source address to said indicated destination address.

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66. (New) The single integrated circuit of claim 63, wherein:

said read/write memory is operable to prioritize requests for access with said first data processor having a highest priority, said second data processor having an intermediate priority and said external interface having a lowest priority.

67. (New) The single integrated circuit of claim 63, further comprising:

a second read/write memory connected to said second data processor, whereby said second data processor is capable of reading from and writing to said second read/write memory and said first data processor is not capable of either reading from or writing to said second read/write memory.

68. (New) The single integrated circuit of claim 63, wherein:

said first data processor is a digital signal processor (DSP); and

said second data processor is a reduced instruction set computer (RISC) processor.

69. (New) A single integrated circuit comprising:

a first data processor including

a first program counter (2903) storing an address of a next instruction,

a first opcode register (2911) storing a current instruction,

first data processing units (2902, 2905, 2906, 2907, 2908, 2909, 2910) capable of data processing,

a first control logic (2904) connected to said opcode register for control of said first data processing units corresponding to said current instruction stored in said first opcode register according to a first instruction set;

a first read/write instruction memory connected to said first data processor storing instructions in said first instruction set, said first data processor operating in accordance with instructions in said first instruction set recalled from said first instruction memory;

a second data processor including

a second program counter (3100) storing an address of a next instruction,

a second opcode register (3105) storing a current instruction,

second data processing units (3301, 3302, 3303, 3304) capable of data processing,

a second control logic (3002) connected to said opcode register for control of said second data processing units corresponding said current instruction stored in said second opcode register according to a second instruction set, said second data processing units having a different mapping of instructions to controlled operations than that of said first instruction set;

a second read/write instruction memory connected to said second data processor storing instructions in said second instruction set, said second processor operating in accordance with instructions in said second instruction set recalled from said second instruction memory; and

a read/write data memory connected to said first data processor and said second data processor, whereby both said first

data processor and said second processor are capable of reading from and writing to said read/write data memory.

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70. (New) The single integrated circuit of claim 69, wherein:

said first data processor further includes a first data register file (2901) connected to said first data processing units for temporarily storing data; and

said second data processor further includes a second data register file (3300) connected to said second data processing units for temporarily storing data.

71. (New) The single integrated circuit of claim 69, wherein:

said read/write data memory is operable to prioritize requests for access with said first data processor having a highest priority and said second data processor having a lowest priority.

72. (New) The single integrated circuit of claim 69, further comprising:

a second read/write data memory connected to said second data processor, whereby said second data processor is capable of reading from and writing to said second read/write data memory and said first data processor is not capable of either reading from or writing to said second read/write data memory.

73. (New) The single integrated circuit of claim 69, wherein:

said first data processor is a digital signal processor (DSP); and

said second data processor is a reduced instruction set computer (RISC) processor.

74. (New) The single integrated circuit of claim 69, wherein:

said first and second data processors are capable of independent operations on disjoint instructions and data sets.

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75. (New) The single integrated circuit of claim 69, wherein:

said first read/write instruction memory being configured as a first instruction cache;

said second read/write instruction memory being configured as a second instruction cache;

said first data processor further including a first instruction cache logic circuit (3101) connected to said program counter and said first instruction cache for determining if an instruction corresponding to the address stored in said first program counter is stored in said first instruction cache;

said second data processor further including a second instruction cache logic circuit connected to said second program counter and said second instruction cache for determining if an instruction corresponding to the address stored in said second program counter is stored in said second instruction cache; and

an external interface (11) connected to said first data processor, said second data processor, said first instruction cache and said second instruction cache and connectable to memory (15) external to said single integrated circuit, said external interface transferring an instruction corresponding to the address stored in said first program counter from said memory external to said single integrated circuit to said first instruction cache if said first instruction cache logic circuit determines said instruction is not stored in said first instruction cache, and said external interface transferring an instruction corresponding to the address stored in said second program counter from said memory external to said single integrated circuit to said second instruction cache if said second instruction cache logic circuit determines the instruction is not stored in said second instruction cache.